DIGITAL & ANALOG IC DESIGN
(EC503)

Objective of the Course :
The objective of this course is to teach analog integrated circuit design using today's technologies and in particular CMOS technology. Also the student will be introduced to implement practical digital functional blocks using VHDL / Verilog.

UNIT - I
Operational Amplifiers: General considerations one – state op-amps, two stage op-amps – gains boosting stage – comparison – I/P range limitations slew rate.
Current Mirrors ad Single Stage Amplifiers: simple CMOS, BJT current mirror, Cascode Wilson Wilder current mirrors. Common Source amplifier source follower, common gate amplifier
Noise: Types of Noise – Thermal Noise – flicker noise – Noise in opamps – Noise in common source stage– noise band width.

UNIT - II
Phased Locked Loop Design: PLL concepts – The phase locked loop in the locked condition –Integrated circuit PLLs – phase Detector – voltage controlled oscillator – case study: Analysis of the 560 B Monolithic PLL.
Switched Capacitors Circuits: Basic Building blocks op-amps capacitors – switches – no overlapping clocks – Basic operations and analysis – resistor equivalence of a switched capacitor – parasitic sensitive integrator – parasitic insensitive integrators – signal flow graph analysis – First order filters – switch sharing fully differential filters – charged injections – switched capacitor – gain circuits – parallel resistor – capacitor circuit – presettable gain cuicuit – other switched capacitor circuits – full wave rectifier –peak detector – sinusoidal oscillator.

UNIT - III
Logic Families & Charactristics: CMOS, TTL, ECL, logic families – CMOS / TTL,interfacing, comparison of logic families.
Combinational Logic Design Using VHDL: VHDL modeling for decoders, 4encoders,multipluxers, comparators, adders and subtractors.
Sequential IC Deisgn Using VHDL: VHDL modeling for latches, flip flaps, counters, shift registers,FSMs.

UNIT - IV
Digital Integraded System Building Blocks: Multiplexers and decoders – Barrel shifters– counters digital single bit adderMEMORIES: ROM: Internal structure 2D decoding commercial types timing and applicationsCPLD: XC 9500 series family CPLD architecture, functional block internal architecture. I/O block – internal structure.
FPGA: Conceptual of view of FPGA – classification based on CLB arrangement – programming technologies – XC 4000 series family architecture – CLB internal architecture – I/O block architecture.

UNIT - V
Comporators: Using an op-amp for a comparator – charge injection errors – latched comparator.
Nyquist Rate D/A Converters: Decoder based converter resistor storing converters, folded resister string converter – Binary scale converters – Binary weighted resistor

converters – Reduced resistance ratio ladders – R-2R based converters – Thermometer code current mode D/A converters.

Nyquist Rate A/D Converters: Integrating converters – successive approximation converters –DAC based successive approximation – flash converters time interleaved A/D converters.

Text Books :

1. Analog Integrated Circuit Design by David A.Johns, Ken Martin, John Wiley & Sons.
2. Analysis and Design of Analog Integrated Circuits, by Gray, Hurst Lewis, Meyer. John Wiley &Sons.
3. Design of Analog CMOS Integrated Circuits, Behzad Razavi. TMH

Reference Books :

1. Ken Martin, Digital Integrated Circuit Design Oxford University, 2000.
2. John F Wakerly, "Digital Design Principles & Practices", Pearson Education & Xilinx Design Series,3rd ed., 2002.
3. Samir Palnitkar, "Verilog HDL-A Guide to Digital Design and Synthesis", Prentice Hall India,(2000).
4. Douglas J Smith, "HDL Chip Design, a Practical Guide for Designing, Synthesizing and Simulating, ASICs and FPGAs using VHDL or Verilog, Doone Publications, 1999.