17ES015 SYSTEM ON-CHIP DESIGN

Hours Per Week :

L	T	P	C
4	-	-	4

Total Hours :

L	T	P
60	-	-

WA/RA	SSH/HSH	CS	SA	S	BS
15	30	-	5	5	-

Course Objectives:

- To understand the concepts of System on Chip Design methodology for Logic and Analog Cores.
- To understand the concepts of System on Chip Design Validation.
- To understand the concepts of SOC Testing.

Course Outcomes:

- Upon successful completion of this course student should be able to: understand about SoC Design Methodology.
- Ability to understand the design of different embedded memories.
- SoC Design Validation and Testing Concepts can be understood.

SKILLS:

- He can know the different Bus protocols/architecture scan become an Expert in the following areas:
- Low Power, Security, Networking, Wireless, Flash Memory, Graphics, DSP.
- Good understanding of entire design flow, from RTL to GDS High RTL coding skills.

UNIT – I

Introduction- System tradeoffs and evolution of ASIC Technology- System on chip concepts and methodology – SoC design issues -SoC challenges and components.

UNIT – II

Design Methodological For Logic Cores- SoC Design Flow – On-chip buses –Design process for hard cores –Soft and firm cores – Core and SoC design examples.

UNIT – III

Design Methodology for Memory and Analog Cores- Embedded memories –Simulation modes Specification of analog circuits – A to D converter –Phase locked loops –High I/O.

UNIT – IV

Design Validation- Core level validation –Test benches –SoC design validation – Co simulation – hardware/ Software co-verification. Case Study: Validation and test of systems on chip.

UNIT – V

SoC Testing- SoC Test Issues –Cores with boundary scan –Test methodology for design reuse– Testing of microprocessor cores – Built in self-method –testing of embedded memories. Case Study: Integrating BIST techniques for on-line SoC testing.

TEXT BOOKS:

1. RochitRajsunah, System- on - a -chip: Design and Test, Artech House, 2007.

2. PrakashRaslinkar, Peter Paterson &Leena Singh, System-on-a-chip verification: Methodology and Techniques, Kluwer Academic Publishers, 2000.

REFERENCE BOOKS:

1. M.Keating, D.Flynn, R.Aitken, A, GibbonsShi, Low Power Methodology Manual for System-on-Chip Design Series: Integrated Circuits and Systems, Springer, 2007.

2. L.Balado, E. Lupon, Validation and test of systems on chip, IEEE conference on ASIC/SOC,1999.

3. A.Manzone, P.Bernardi, M.Grosso, M. Rebaudengo, E. Sanchez, M.SReorda, Centro Ricerche Fiat, Integrating BIST techniques for on-line SoC testing, IEEE Symposium on On-Line testing, 2000

ACTIVITIES:

- VHDL MODEL OF SMART SENSOR.
- VHDL Environment for Floating point Arithmetic Logic Unit - ALU Design and Simulation.
- DESIGN OF AN ON-CHIP PERMUTATION NETWORK FOR MULTIPROCESSOR SOC.
- Design and Synthesis of a Field Programmable CRC Circuit Architecture.
- Design of FPGA based 32-bit Floating Point Arithmetic Unit and verification of its VHDL code using MATLAB..