17VL012 ASIC

Hours Per Week :

L	T	P	C
4	-	-	4

Total Hours :

L	T	P
60	-	-

WA/RA	SSH/HSH	CS	SA	S	BS
15	30	-	5	5	-

Course Objectives:

- To prepare the student to be an entry-level industrial standard ASIC or FPGA designer.
- To give the student an understanding of issues and tools related to ASIC/FPGA design and implementation.
- To give the student an understanding of basics of System on Chip and platform based design.

Course Outcomes:

Upon successful completion of this course student should be able to:

- Demonstrate VLSI tool-flow and appreciate FPGA architecture.
- Understand the issues involved in ASIC design, including technology choice, design management, tool-flow, verification, debug and test, as well as the impact of technology scaling on ASIC design.
- Understand the algorithms used for ASIC construction.
- Understand the basics of System on Chip, on chip communication architectures like AMBA, AXI and utilizing Platform based design.
- Appreciate high performance algorithms available for ASICs IC.

SKILLS:

- Digital ASIC design and verification techniques
- Detailed knowledge of the complete ASIC design flow

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UNIT - I

Types of ASICs, VLSI Design flow, Programmable ASICs - Antifuse, SRAM, EPROM, EEPROM based ASICs. Programmable ASIC logic cells and I/O cells. Programmable interconnects. Latest Version - FPGAs and CPLDs and Soft-core processors.

UNIT - II

Trade off issues at System Level: Optimization with regard to speed, area and power, asynchronous and low power system design. ASIC physical design issues, System Partitioning, Power Dissipation, Partitioning Methods.

UNIT - III

ASIC floor planning, Placement and Routing.

UNIT - IV

System-On-Chip Design - SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures, On-Chip Communication Architecture Standards, Low-Power SoC Design.

UNIT - V

High performance algorithms for ASICS/ SoCs as case studies – Canonic Signed Digit Arithmetic, KCM, Distributed Arithmetic, High performance digital filters for sigma-delta ADC, USB controllers, OMAP

ACTIVITIES:

- Design a SRAM memory cell.
- Floor planning, routing and placing of adder in ASIC.
- Design of digital filter of ADC.

TEXT BOOKS

1. M.J.S. Smith,"Application Specific Integrated Circuits", Pearson, 2003
2. H.Gerez, "Algorithms for VLSI Design Automation", John Wiley, 1999.

REFERENCE BOOKS

1. J..M.Rabaey, A. Chandrakasan, and B.Nikolic, "Digital Integrated Circuit Design Perspective (2/e)", PHI 2003.
2. D. A.Hodges, "Analysis and Design of Digital Integrated Circuits (3/e)", MGH 2004.
3. Hoi-Jun Yoo, KangminLeeand Jun Kyong Kim, "Low-Power NoC for High-Performance SoC Design", CRC Press, 2008.
4. S.Pasricha and N.Dutt," OnChip Communication Architectures System on Chip Interconnect, Elsveir", 2008.