Design of a CNTFET based Low Power Ternary Content Addressable Memory

PROJECT REPORT

Submitted in the fulfilment of the requirements for

the award of the degree of

Bachelor of Technology
in
Electronics and Communication Engineering

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VIGNAN'S
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(Deemed to be University)
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VIGNAN'S FOUNDATION FOR SCIENCE, TECHNOLOGY AND RESEARCH
(Deemed to be University)

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May 2024

CERTIFICATE

This is to certify that project report entitled **"Design of a CNTFET based Low Power Ternary Content Addressable Memory"** that is being submitted by Thumma Mariya Manasa [201FA05042], Monu Kumar [201FA05092] and Alla Sai Rakesh [201LA05032] in fulfilment for the award of B. Tech degree in Electronics and Communication Engineering, Vignan's Foundation for Science Technology and Research University, is a record of bonafide work carried out by them under the guidance of Dr. V. Aswini of ECE Department.

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Associate Professor

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Signature of Head of the Department
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Professor & HoD ECE

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DECLARATION

We hereby declare that the project report entitled **"Design of a CNTFET based Low Power Ternary Content Addressable Memory"** is being submitted to Vignan's Foundation for Science, Technology and Research (Deemed to be University) in fulfilment for the award of B. Tech degree in Electronics and Communication Engineering. The work was originally designed and executed by us underthe guidance of Dr. V. Aswini at the Department of Electronics and CommunicationEngineering, Vignan's Foundation for Science Technology and Research (Deemed to be University) and was not a duplication of work done by someone else. We hold the responsibility of the originality of the work incorporated into this project report.

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ABSTRACT

This project describes a new Ternary Content Addressable Memory (TCAM) cell design based on carbon nanotube field-effect transistors (CNTFETs). A Content Addressable Memory (CAM) is a memory that implements the lookup-table function in a single clock cycle using dedicated comparison circuitry. CAMs are especially popular in network routers for packet forwarding and packet classification, but they are also beneficial in a variety of other applications that require high-speed table lookup. Apart from the high speed, the main CAM-design challenge is to reduce power consumption associated with the large amount of parallel active circuitry, without sacrificing speed or memory density. The project aims to design a TCAM cell with low power consumption and high which helps in reducing the overall power consumption of the CAM architecture with improved performance. The circuits are implemented in Cadence using CNTFET 32nm technology with supply voltage 0.9v. The Proposed design is yielding good results in terms of power and delay, and the results are compared with the existing circuits in literature.

Major Design (Final Year Project Work) Experience Information

Student Group	T. Mariya Manasa (201FA05042)	Monu Kumar (201FA05092)	A. Sai Rakesh (211LA05032)
Project Title	Design of a CNTFET based low power Ternary Content Addressable Memory		
Program Concentration Area	Low power circuit design		
Constraints - Examples			
Economic	Fixed budget (limited), cost-effective system design		
Environmental	Friendly		
Sustainability	Achieves sustainability by reducing the overall power consumption of a device		
Manufacturability	Yes		
Ethical	Followed the standard professional ethical		
Health and Safety	Guidelines are followed		
Social	Used in network routers		
Political	None		
Other			
Standards			
1. IEEE 1801-2009/2018	IEEE standard for design and verification of low power energy aware electronic systems		
Previous Courses Required for the major design experience	1. Electronic Devices and Circuits 2. VLSI design		

Supervisor **Project Co-Ordinator** **Head of the department ECE**

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LIST OF ACRONYMS

BL	Bit Line
BCAM	Binary Content Addressable Memory
CAM	Content Addressable Memory
CMOS	Complementary Metal-Oxide Semiconductor
CNTFET	Carbon Nano Tube Field Effect Transistor
EDA	Electronics Device Automation
FPGA	Field Programmable Gate Array
IC	Integrated Circuit
ML	Match Line
PDP	Power Delay Product
RF	Radio Frequency
SL	Search Line
TCAM	Ternary Content Addressable Memory
WL	Word Line

CHAPTER 1
INTRODUCTION

1.1 INTRODUCTION

The primary function of any memory system is writing and reading the lookup data. Random access memory (RAM) is a volatile memory. It searches lookup table data serially in the memory array, and it requires more clock cycles to search the data. Thus, for large capacity memory, RAM is not suitable for high-speed search. Content addressable memory (CAM) is a particular type of computer memory, also known as associative memory. From the functionality point of view, RAM is an inverse of CAM. RAM reads the content of stored memory based on the address match whereas CAM reads the content of stored memory based on the content match [1]. CAM cell can perform all the functions of RAM. It requires comparison circuitry in addition, to get miss/match case at ML, when search input compares with a stored data. CAM surmounts all memory search algorithms for high-speed search. CAM with a large capacity word well in various types of applications that involve searching of lookup table data with high speed. CAM is utilized in wide variety of high-speed applications like network routers, cache controllers, image-processing, gray coding and so on [2]. However, the parallel search lookup table within a single clock cycle offers high search speed and switching activity. As a result, CAM operates with high performance but suffers from high power consumption. Thus, research concentrates in CAM designing to minimize power without degrading the performance. CAMs can be divided into two categories: (i) binary CAMs and (ii) ternary CAMs (TCAMs) [3]. A binary CAM can store and search binary words (made of '0's and '1's). Thus, binary CAMs are suitable for applications that require only exact-match searches. A more powerful and feature rich TCAM can store and search ternary states ('1', '0', and 'X'). The state 'X', also called 'mask' or 'don't care', can be used as a wild card entry to perform partial matching.

The CMOS technology is scaled down to achieve high chip density, low power consumption, high speed with greater performance. But due to the continuous scaling, the leakage current increases in the CMOS devices. The further scaling of CMOS i,e below nm, faces major technology limitations which may restrict in terms of size, power consumption and speed. Therefore, CMOS technology in the deep submicron level has reached saturation mainly because of the leakage current and short channel effect. CNTFETs are therefore considered as the promising alternative that can overcome the limits of silicon-based technology [4]. CNTs can be conducted either as semiconductors or metal based on their chirality. The major benefit of CNTFETs over MOSFETs is, that the CNTFET's threshold voltage can be determined with the diameter of its

CNTs used through which the design of digital circuits can be made flexible than the MOSFETs [5].

This project aims to design a TCAM cell with minimized power without degrading the performance. To achieve the low power consumption of a device, IEEE standard for design and verification of low power energy aware electronic systems (IEEE 1801-2009/2018) is used. The design can achieve sustainability by reducing the overall power consumption of a device by following the ethical, health and safety guidelines.

1.2 MOTIVATION

The Motivation for this project, "Design of a CNTFET-Based Low Power Ternary Content Addressable Memory", arises from the critical need to enhance the performance and efficiency of memory systems in modern computing applications. Ternary Content Addressable Memory (TCAM) is frequently used in high-speed search applications such as network routers, cache memory, and data compression techniques because of its ability to execute quick lookups by searching the full memory contents in a single clock cycle. However, typical CMOS-based TCAM systems have major hurdles, largely due to excessive power consumption and scaling restrictions. These issues become more obvious as the demand for quicker and more efficient data processing increases.

As CMOS technology approaches its physical and material limits, issues such as short channel effects, leakage currents, and high-power density hinder the further miniaturization and performance enhancement of CMOS-based TCAMs. This scenario necessitates the exploration of alternative technologies that can offer better performance and energy efficiency. Carbon Nanotube Field-Effect Transistors (CNTFETs) present a promising solution due to their unique electrical properties, including high carrier mobility, ballistic transport, and low power dissipation. These characteristics make CNTFETs an ideal candidate for designing low-power and high-performance electronic circuits, including TCAMs.

The increasing focus on energy-efficient computing further motivates this research. With growing concerns about energy consumption and its environmental impact, developing memory technologies that reduce power usage without compromising performance is crucial. CNTFET-based designs have the potential to significantly lower power requirements, making them suitable

for next-generation low-power memory solutions. Additionally, the scalability of CNTFET technology supports the ongoing miniaturization trend in electronic systems, aligning with Moore's Law and the need for more compact and efficient devices.

Moreover, reducing power consumption in memory devices directly contributes to sustainability by minimizing heat generation and the associated cooling demands. This leads to overall energy savings and a smaller carbon footprint for data centers and electronic devices, addressing both economic and environmental concerns. The primary objective of this project is to design and evaluate a low power TCAM using CNTFET technology. This involves developing an optimized TCAM architecture that leverages the advantages of CNTFETs to achieve low power consumption and high-speed operation. Comprehensive simulations and analyses will be conducted to compare the proposed CNTFET-based TCAM with conventional CMOS-based designs in terms of power, speed, and area. The research also aims to implement a prototype to validate the theoretical and simulation results, demonstrating the feasibility and advantages of the proposed design.

1.3 OBJECTIVE

1.3.1 BROAD OBJECTIVE:

To design and develop a Ternary Content Addressable Memory (TCAM) using Carbon Nanotube Field-Effect Transistor (CNTFET) technology to achieve significant reductions in power consumption while enhancing performance.

1.3.2 SPECIFIC OBJECTIVE:

1. To design an optimized Ternary Content Addressable Memory (TCAM) architecture utilizing Carbon Nanotube Field-Effect Transistor (CNTFET) technology to achieve significant reductions in power consumption.
2. To conduct simulations and analyses to evaluate the power efficiency, speed, and area utilization of the CNTFET-based TCAM design.

1.4 CADENCE VIRTUOSO

View other drafts Cadence Virtuoso is a comprehensive suite of electronic design automation (EDA) tools used for integrated circuit (IC) design and verification. It provides a wide range of capabilities for designing, simulating, and laying out ICs, from small analog circuits to complex digital systems. Virtuoso is a popular choice for IC designers due to its powerful features, ease of use, and wide industry support.

The purpose of Cadence Virtuoso is to enable engineers to: Design and verify integrated circuits (ICs) Create high-performance, reliable ICs Meet the stringent requirements of IC manufacturing Design ICs for a wide range of applications, including consumer electronics, medical devices, and automotive systems Virtuoso is used in all stages of the IC design process, from initial schematic capture to final layout verification.

It includes tools for: Schematic capture: Creating and editing circuit schematics Simulation: Simulating circuit behaviour to verify functionality and performance Layout: Placing and routing transistors and other components on the chip Verification: Checking the layout for design rule violations and ensuring that it meets all electrical and timing requirements Virtuoso is also integrated with a variety of other EDA tools, such as Cadence's IC Compiler and Design Compiler, to provide a complete IC design flow.

This allows designers to seamlessly transition between different stages of the design process and use the best tools for each task. Here are some of the key benefits of using Cadence Virtuoso: Increased productivity: Virtuoso's ease of use and powerful features can help designers to create ICs more quickly and efficiently. Improved design quality: Virtuoso's comprehensive verification tools can help to ensure that ICs meet all electrical and timing requirements. Reduced time to market: Virtuoso can help to reduce the time it takes to bring ICs to market. Lower development costs: Virtuoso can help to reduce the cost of developing ICs.

Overall, Cadence Virtuoso is a valuable tool for IC designers who want to create high performance, reliable ICs quickly and efficiently. In addition to the above, here are some specific examples of how Cadence Virtuoso is used: Analog IC design: Virtuoso is used to design a wide range of analog ICs, including operational amplifiers, filters, and voltage regulators.

CHAPTER 2

TERNARY CONTENT ADDRESSABLE MEMORY

2.1 TCAM CELL OPERATION

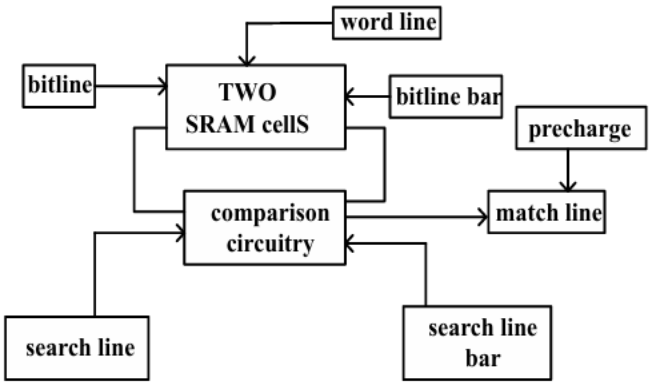

Figure 2.1: Block Diagram of TCAM

TCAM cells are designed to store and search lookup table data within a single clock cycle. TCAM cells use Two SRAM cells to store ternary value don't care X other than 0 or 1. In TCAM for bit comparison, circuitry is based on the type of application. The bit comparison in TCAM cell design is logically equivalent to XOR or XNOR of the stored bit and search bit. The transistors in the comparison circuitry are designed with typically minimum sized to maintain high cell density. TCAM operation is performed in two stages precharge phase and evaluation phase [6]. TCAM cell operation begins with loading the search input through search lines followed by pre-charging match line, once the match line is pre-charge it temporarily disconnects match line from ground. Next, search data is broadcast through search line to compare with the store data. While comparing stored bit and the search bit if there is a match indicates match state then match line isolated from the discharge discharge path otherwise it indicates miss state then match line connected to ground.

2.2 TCAM ARRAY

A Ternary Content Addressable Memory (TCAM) array is an integrated circuit used for high-speed search operations. Unlike traditional memory systems, which retrieve data based on a given address, a TCAM array compares input search data against a stored dataset and returns the address of the matching data, if any. This makes TCAM arrays particularly useful in applications requiring rapid data lookup, such as networking equipment for routing and packet forwarding, database acceleration, and data compression.

In a TCAM array, multiple TCAM cells are organized in a grid-like structure with rows and columns. Each row represents a stored data word, and each column corresponds to a specific bit position within those words. The array operates through a two-phase process involving precharging and comparison.

During the precharge phase, the match lines (MLs) for all rows are precharged to a high voltage (Vdd) by activating the precharge transistors. This prepares the match lines for the subsequent comparison phase. Next, during the comparison phase, the search data is simultaneously applied to all rows of the TCAM array through the source lines (SL and SLbar). Each TCAM cell in the array compares the corresponding bit of the search data to its stored bit.

The TCAM cells within each row work together to determine whether the search data matches the stored data. If the data in a particular row matches the search data, the match line for that row remains high. If there is any bit mismatch within a row, the corresponding transistors in the mismatched cells pull the match line low, indicating a mismatch.

The key advantage of a TCAM array is its ability to perform parallel comparisons across all rows simultaneously, enabling rapid data searches in a single clock cycle. This is especially beneficial for applications that require high throughput and low latency [7]. By employing CNTFET technology, the TCAM array can achieve further improvements in power efficiency and operational speed, leveraging the high carrier mobility and low power dissipation characteristics of CNTFETs compared to conventional CMOS technology.

Overall, a TCAM array's parallel search capability and fast operation make it an essential component for modern high-speed data processing systems, significantly enhancing performance in tasks that involve large-scale and frequent data lookups.

2.3 NAND AND NOR TCAM CELLS

2.3.1 NAND TYPE TCAM CELL

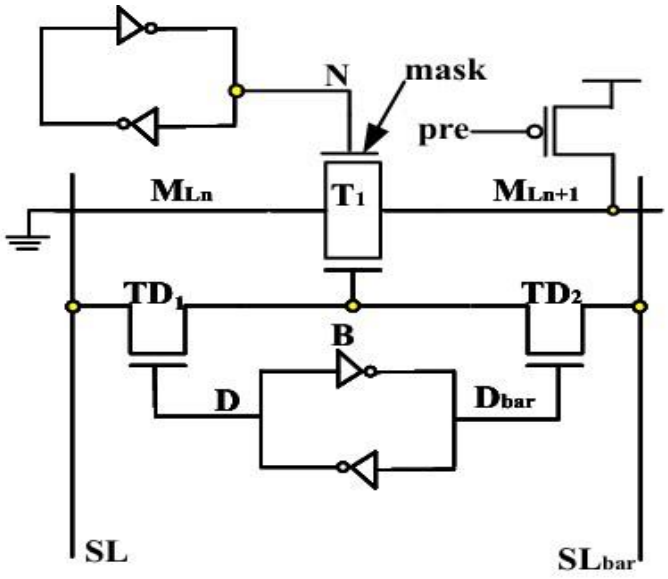

Figure 2.2: NAND type TCAM cell structure

NAND TCAM (Ternary Content Addressable Memory) cell is a fundamental building block in content-addressable memory arrays. Its operation can be described in several steps.

Firstly, the NAND TCAM cell comprises a storage element, typically consisting of two transistors and one resistor, forming a NAND gate configuration. This structure allows for efficient storage of ternary information, where each cell can store one of three states: 0, 1, or X (don't care).

Secondly, during a read operation, the TCAM cell compares its stored data with an input search key. This is achieved by applying the search key to one input of the NAND gate while the stored data is applied to the other input. If there is a match, the output of the NAND gate remains low, indicating a hit. If there is no match, the output goes high, indicating a miss.

Thirdly, in a write operation, the NAND TCAM cell can be programmed to store a specific ternary value. This is accomplished by selectively applying voltages to the control inputs of the transistors within the cell, altering their conductivity and thus the stored data.

Furthermore, the NAND TCAM cell offers advantages such as high density and low power consumption compared to traditional SRAM-based TCAM implementations. Its NAND-based architecture enables compact integration and efficient utilization of silicon area.

In summary, the operation of a NAND TCAM cell involves storing ternary data efficiently, comparing it with input search keys, and enabling read and write operations with low power consumption and high density, making it a versatile and valuable component in content-addressable memory systems.

2.3.2 NOR TYPE TCAM CELL

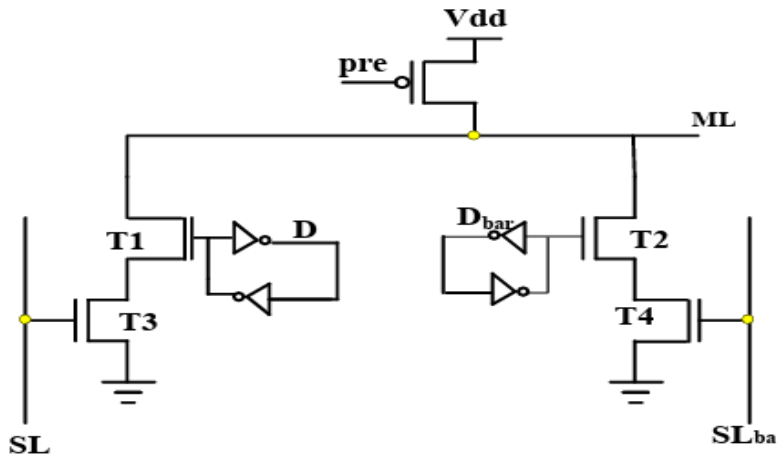

Figure 2.3: NOR type TCAM cell structure.

The NOR TCAM (Ternary Content Addressable Memory) cell serves as a core element within content-addressable memory arrays. Its operation can be delineated into several key steps.

Firstly, the NOR TCAM cell is constructed using a combination of transistors and resistors, typically configured in a NOR gate arrangement. This design allows for efficient storage of ternary data, where each cell can represent one of three states: 0, 1, or X (don't care).

Secondly, during a read operation, the stored data within the NOR TCAM cell is compared with an input search key. This comparison is facilitated by applying the search key to one input of the NOR gate while the stored data is applied to the other input. If there is a match between the search key and the stored data, the output of the NOR gate remains low, signalling a hit. Conversely, if there is no match, the output goes high, indicating a miss.

Thirdly, in a write operation, the NOR TCAM cell can be programmed to store a specific ternary value. This is accomplished by selectively applying voltages to the control inputs of the transistors within the cell, thereby altering their conductivity and consequently modifying the stored data.

Moreover, the NOR TCAM cell offers advantages such as high integration density and low power consumption when compared to traditional SRAM-based TCAM implementations. Its NOR-based architecture enables efficient utilization of silicon real estate and facilitates compact integration within memory arrays.

In summary, the operation of a NOR TCAM cell encompasses efficient storage and retrieval of ternary data, enabling read and write operations with low power consumption and high integration density [8]. These characteristics make the NOR TCAM cell a versatile and valuable component in content-addressable memory systems.

CHAPTER 3

LITERATURE SURVEY

LITERATURE SURVEY

3.1 EXISTING WORK-1

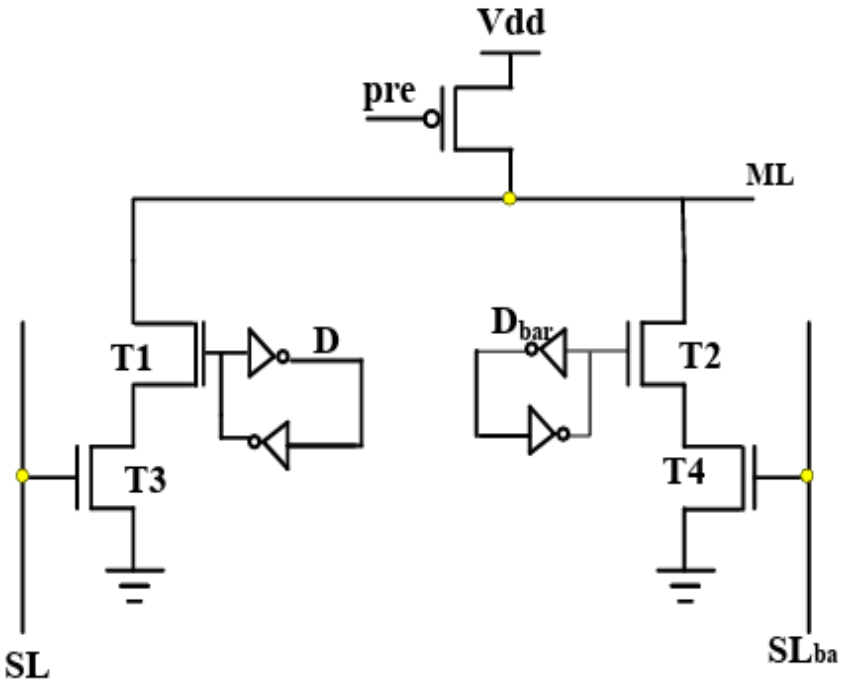

Figure 3.1 Existing Work-1

TCAM is encoded into two its D and Dbar which need not be complementary. These two bits are connected to pull down path independently. Second SRAM is used in TCAM NOR cell design to store a ternary value. TCAM NOR cell store X value by setting D and Dbar to logic 1 which forces the NOR cell to match by disconnecting both pull down paths from the ground despite the inputs. Searching for an X in TCAM NOR cell is possible by setting SL and SLbar to logic Low [9].

Table 3.1: Truth Table EW-1

Q1	Q2	SL	SLb	ML
0	1	0	1	Match
0	1	1	0	Miss
1	0	0	1	Miss
1	0	1	0	Match
1	1	X	X	Match

3.2 EXISTING WORK-2

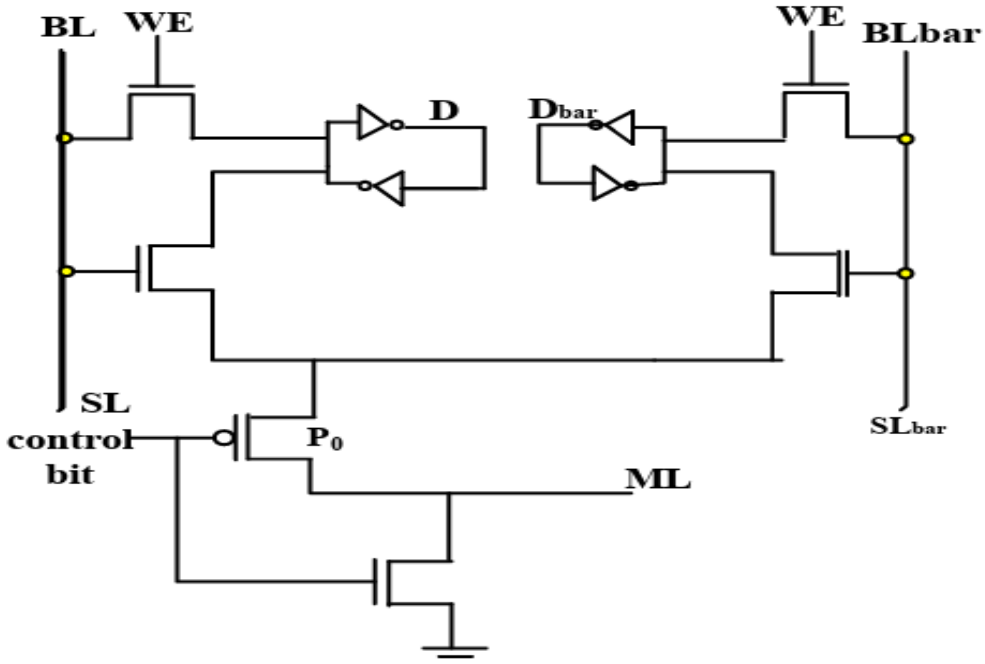

Figure 3.2: Existing Work-2

Normally CAM operation begins with pre-charging then by evaluation. It is observed that in precharge phase power wastage is more in CAM, because of short circuit current and charge sharing problems, and this occurs when there is a mismatch between the stored bit and search bit. To overcome this problem BCAM cell is modified to avoid precharge phase completely. They proposed TCAM based precharge free CAM cell is shown in Figure 3.2. Here both control bit and pull-down transistor help in avoiding the precharge phase. To operate the cell in precharge free,

the control bit is set to null which makes pull down transistor off. Depending on match and miss match between stored bit and search bit match line remain high or low [9].

Table 3.2: Truth Table EW-2

Q1	Q2	SL	SLb	ML
0	1	0	1	Match
0	1	1	0	Miss
1	0	0	1	Miss
1	0	1	0	Match
1	1	X	X	Match

3.3 EXISTING WORK-3

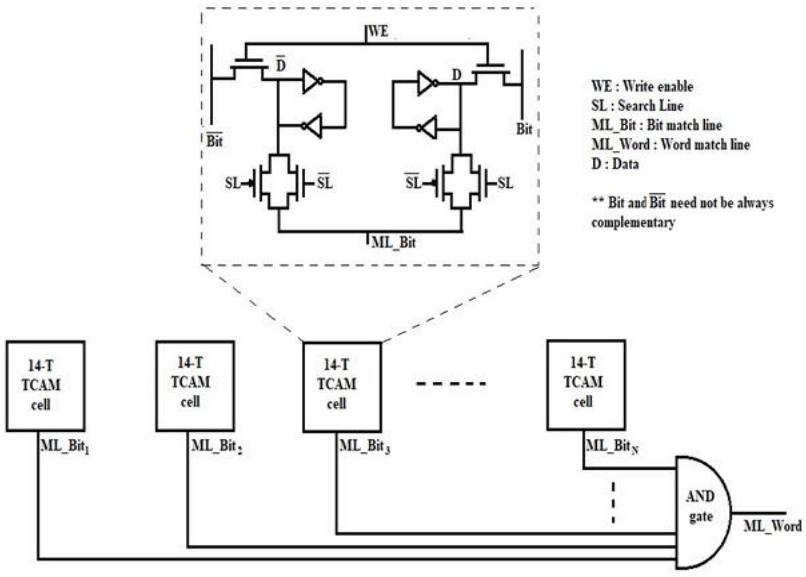

Figure 3.3: Existing Work-3

Transmission gate offering rail to rail voltage swing can be used instead of the pass transistors in the single CAM cell, with a moderate increase in the rising propagation delay due to the additional parasitic capacitance introduced in the signal path. The individual match lines, instead of forming a series pass transistor path, are directly given to a CMOS AND gate, whose output then becomes the match-line for a word. In the existing architecture as shown in Fig. 3.3,

the main aim is to eliminate the power consumption due to pre-charging and pulling the MLs to ground before the start of every search cycle which is achieved. The existing architecture eliminates the need for CB signal, and hence results in improving the frequency of search operations [10].

Table 3.3: Truth Table EW-3

Q1	Q2	SL	SLb	ML
0	1	0	1	Match
0	1	1	0	Miss
1	0	0	1	Miss
1	0	1	0	Match
1	1	X	X	Match

CHAPTER 4

PROPOSED DESIGN

4.1 PROPOSED TCAM CELL

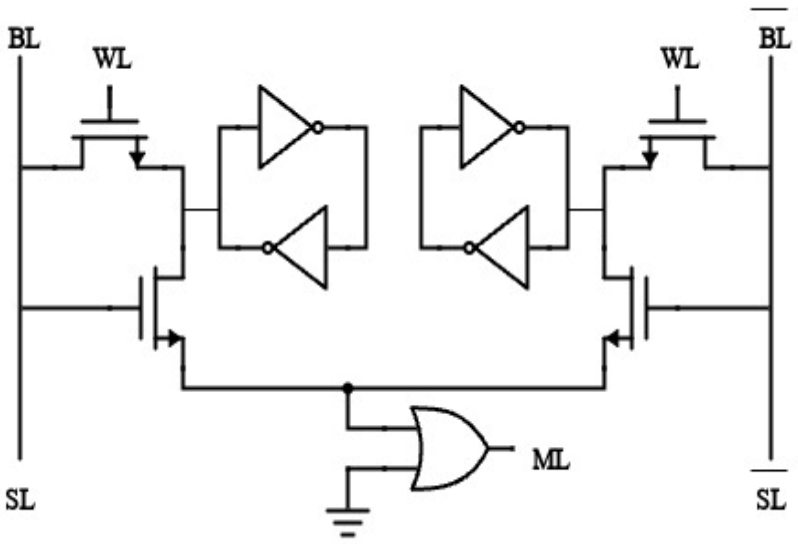

Figure 4.1: Precharge free OR logic type TCAM cell structure

Normally TCAM operation begins with pre-charging then by evaluation. It is observed that in precharge phase power wastage is more in TCAM, because of short circuit current and charge sharing problems, and this occurs when there is a mismatch between the stored bit and search bit. To overcome this problem TCAM cell is modified to avoid precharge phase completely. We have proposed TCAM based precharge free CAM cell is shown in Figure 4.1. In a typical CAM operation, a precharge phase is used to set the match line to a known state before comparison. In this case, without a precharge phase, the match line state directly reflects the comparison result. If the stored data in the cell matches the search data, the match line (ML) remains high. If any bit does not match, the mismatch transistors will pull the match line low. Here we have used the OR gate which is connected to output of the match line.

OR gate helps us to avoid the pre-charge phase and pull-down transistor. To operate the TCAM cell OR gate relates to transistors and output of the gate is worked as the match line. To combine the results of multiple cells, an OR gate is used. The output of each match line from individual cells is fed into an OR gate. The OR gate will output a high signal if any of the match lines are high, indicating at least one match across the cells. Conversely, the OR gate output will be low

only if all match lines are low, indicating no match. OR gate reduced power consumption and significantly increased the frequency of the search operation this may cause the delay will decrease. This Precharge free OR logic type TCAM design are followed IEEE Standard 1801-2009/2018. IEEE standard for design and verification of low power energy aware electronic systems.

Table 4.1: Truth Table Pre charge free OR logic type TCAM.

Q1	Q2	SL	SLb	ML
0	1	0	1	Match
0	1	1	0	Miss
1	0	0	1	Miss
1	0	1	0	Match
1	1	X	X	Match

4.2 SIMULATION RESULTS

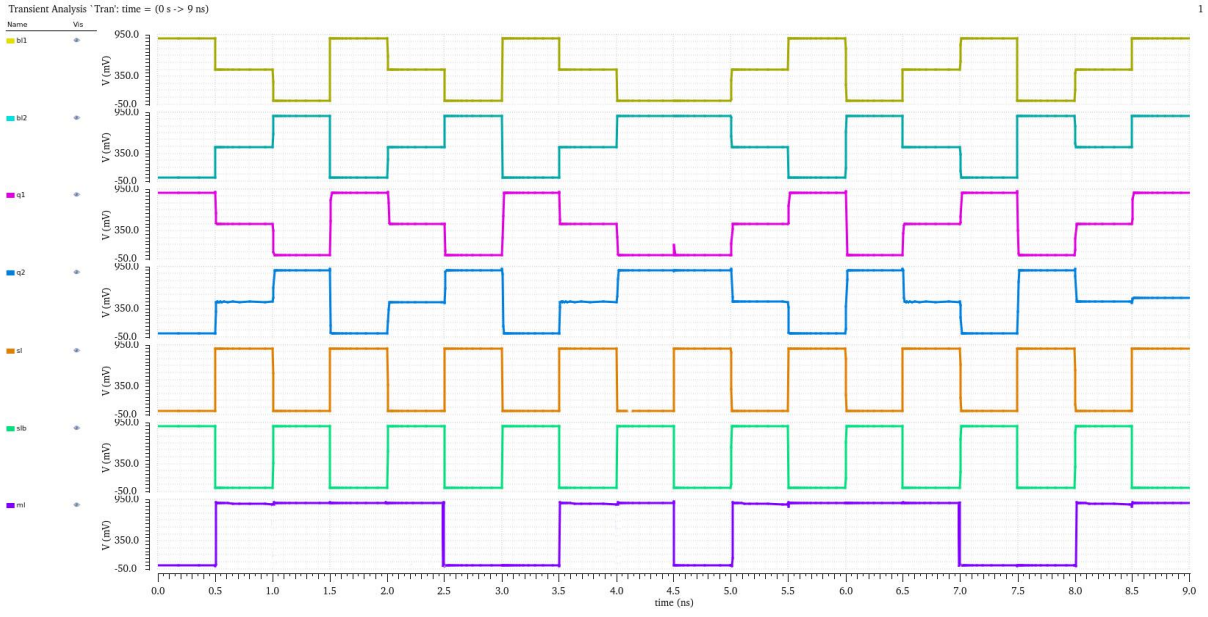

Figure 4.2: Output Wave Form

With the help of Cadence Virtuoso Tool which includes 32nm technology we achieved the output wave form.

4.3 COMPARATIVE ANALYSIS:

Table 4.3: Comparison Table

Parameters	**Existing Work-1**	**Existing Work-2**	**Existing Work-3**	**Proposed Output**
Power(Pw)	288.4	283.5	271.6	266.6
Delay (ns)	14.7	10.6	34.6	5.6
PDP (J)	$4.24x10^{\wedge-21}$	$3.005x10^{\wedge-21}$	$9.47x10^{\wedge-21}$	$1.5x10^{\wedge-21}$

With the help of these important parameters, we have designed the TCAM which benefits in low-power consumption and low-delay. Compared to the above existing works the proposed design offers reduction in power and minimization in search delay.

CHAPTER 5

CONCLUSION & FUTURE SCOPE

5.1 CONCLUSION

This project demonstrates the successful design of a CNTFET-based low power ternary content addressable memory (TCAM), showcasing the remarkable potential of CNTFET technology. CNTFETs offer outstanding performance and durability while significantly reduction in power consumption, making them an ideal choice for modern memory applications.

5.2 FUTURE SCOPE

In future TCAM architecture can be modified to further improve delay and power.

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