## 22CS202 DIGITAL LOGIC DESIGN

Hours Per Week :

| L | T | P | C |
| :--- | :--- | :--- | :--- |
| 2 | 2 | 0 | 3 |

PREREQUISITE KNOWLEDGE: Basics of Computers.

## COURSE DESCRIPTION AND OBJECTIVES:

This course introduces the basic knowledge on number systems, analysis and design of combinational and sequential circuits. The course mainly focuses on designing digital circuits in optimized manner by using components like decoders, encodes, multiplexers. It also deals with design of sequential circuits and Programmable logic devices.

## MODULE-1

## UNIT-1

$8 L+8 T+0 P=16$ Hours

## INTRODUCTION

Number Systems: Binary Numbers, Number base Conversions, Complements, Binary codes.
Boolean Algebra: Fundamental concepts of Boolean algebra basic theorems and properties.
Gate-Level Minimization: Canonical and standard forms - SOP and POS forms, Logic gates, Algebraic simplification and realization with basic gates and universal gates, The map method - two, three, four variable K map; POS and SOP simplification; Don't care conditions; NAND and NOR implementation.

## UNIT-2

8L+8T+0P=16 Hours

## COMBINATIONAL LOGIC CIRCUITS

Combinational circuits analysis, design procedure; Half adder, Full adder, Half subtractor, Full subtractor, Binary adder/subtractor; BCD adder; Binary multiplier; Magnitude comparator; Decoders; Encoders; Multiplexers; De-Multiplexer.

## PRACTICES:

- Design a combinational circuit with three inputs and one output. The output is 1 when the binary value of the inputs is less than 3 . The output is 0 otherwise.
- Design a combinational circuit with three inputs $x, y, z$ and three outputs $A, B, C$. When the binary inputs is $0,1,2$ or 3 , the binary output is one grater than the input. When the binary input is $4,5,6$, or 7 then the binary output is one less than the input.
- Design a code converter that converts a decimal digit from the 8, 4, $-2,-1$ code to BCD.
- Implement a Full - Adder using 4 X 1 multiplexer.
- Design a $16 \times 1$ Multiplexer with five $4 \times 1$ multiplexer.
- Design a 5-to-32 line decoder with four 3-to-8-line decoders with enable and 2-to-4-line decoder.


## MODULE-2

10L+10T+0P=20 Hours

## CIRCUITS, REGISTERS AND COUNTERS

Sequential Logic Circuits: Latches, Flip-Flops-SR, JK, D, T; Flip-flop conversion; Analysis of sequential circuits; Design procedure.
Registers and Counters: Shift registers; Ripple counters; Synchronous counters.

## SKILLS:

$\checkmark \quad$ Learn different data and number representations.
$\checkmark$ Design of logical circuits using all types of gates.
$\checkmark$ Minimizing of Boolean functions.
$\checkmark$ Design of simple logical circuits

## UNIT-2

## $6 L+6 T+0 P=12$ Hours

## MEMORY AND PROGRAMMABLE LOGIC DEVICES

Random access memory; Read only memory; Programmable logic array; Programmable array logic.

## PRACTICES:

- Design a JK flip-flop using a D flip-flop.
- Design a sequential circuit with two $D$ flip-flops $A$ and $B$ and, one input $x$. When $x=0$, the state of the circuit remains same. When $x=1$, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00 and repeats.
- Design a 4-bit binary synchronous counter with $D$ flip-flop.
- A sequential circuit has two J-K fiip-flops A and B. Two inputs $x$ and $y$, and one output $z$. The flip-flop input equations and circuit output equation are:
$J A=B x+B^{\prime} y^{\prime}$
KA=B' $x y^{\prime}$
$J B=A^{\prime} x$
$K B=A+x y^{\prime}$
$Z=A x^{\prime} y^{\prime}+B x^{\prime} y^{\prime}$
a) Tabulate the state table.
b) Derive the state equations.
- Realize the given two Boolean functions with a PLA:
$\mathrm{F} 1(\mathrm{~A}, \mathrm{~B}, \mathrm{C})=\Sigma(0,1,2,4)$
F2 $(\mathrm{A}, \mathrm{B}, \mathrm{C})=\sum(0,5,6,7)$
F3 $3(A, B, C)=\sum(1,3,4,5,7)$
- Tabulate the PAL programming table for the four Boolean functions listed below. Minimize the numbers of product terms.
$A(x, y, z)=\sum(1,3,5,6)$
$B(x, y, z)=\sum(0,1,6,7)$
$C(x, y, z)=\sum(3,5)$
$D(x, y, z)=\sum(1,2,4,5,7)$.


## COURSE OUTCOMES:

Upon successful completion of this course, students will have the ability to:

| CO <br> No. | Course Outcomes | Blooms <br> Level | Module <br> No. | Mapping <br> with POs |
| :---: | :--- | :---: | :---: | :---: |
| 1 | Apply the knowledge of digital logic concepts to <br> optimize digital circuits. | Apply | 1 | 1 |
| 2 | Apply Boolean algebra rules and karnaugh map <br> method to reduce the Boolean functions. | Apply | 1 | 1,2 |
| 3 | Design Combinational digital circuits for the <br> given problem statement by applying the digital <br> techniques. | Analyze | 1 | 3 |
| 4 | Design and analyze sequential digital circuits for <br> the given problem statement and improve the <br> performance by reducing the complexities. | Analyze | 2 | 3 |
| 5 | Categorize various types of Programmable Logic <br> Devices. | Analyze | 2 | 2 |

## TEXT BOOK:

1. M Morris Mano and Michael D. Ciletti, "Digital Design", 5th Edition, Pearson Education, 2013.

## REFERENCE BOOKS:

1. John F.Wakerly, "Digital Design Principles and Practices", 3rd Edition, Pearson/PHI, 2015
2. Charles H.Roth. "Fundamentals of Logic Design", 6th Edition, Thomson Learning, 2013.
3. John. M Yarbrough, "Digital Logic Applications and Design", Thomson Learning, 2006.
