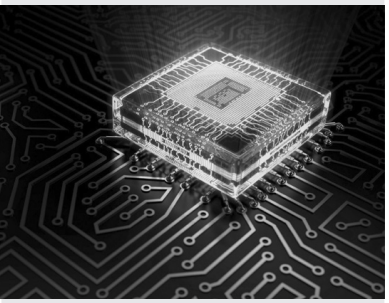

Source: https://machinelearningmedium.com/assets/images/computer-architecture.jpg

22CS205 COMPUTER ORGANIZATION AND ARCHITECTURE

Hours Per Week :

L	T	P	C
2	2	0	3

PREREQUISITE KNOWLEDGE: Digital logic design.

COURSE DESCRIPTION AND OBJECTIVES:

This course covers the basics of modern Computer Organization and Architecture. The emphasis is on understanding the design of computer and its components. The student will learn the concepts of data representation, micro-operations, memory organizations and input output organization.

MODULE-1

UNIT-1 **8L+8T+0P=16 Hours**

INTRODUCTION, RTL, DATA REPRESENTATION AND COMPUTER ARITHMETIC

Introduction, Register Transfer language & Data Representation: Organization and Architecture, Register Transfer, Bus and Memory Transfers, Data Representation-Fixed Point Representation, Floating Point Representation.

Computer Arithmetic: Fixed point arithmetic operations such as Addition and Subtraction, Multiplication Algorithms, Division Algorithms.

UNIT-2 **8L+8T+0P=16 Hours**

MICRO OPERATIONS AND BASIC COMPUTER ORGANIZATION AND DESIGN

Micro operations: Arithmetic Micro operations, Logic Micro Operations, Shift Micro Operations, Arithmetic Logic Shift Unit.

Basic Computer Organization and Design: Instruction Codes, Computer Register, Computer Instructions, Instruction Cycle, Memory – Reference Instructions. Register Reference Instructions, Input –Output and Interrupt.

PRACTICES:

- Design a Common bus system for eight registers with eight bits each using multiplexers.
- Design a Common bus system for four registers with four bits each using three state gate buffers.
- A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.
  How many selection inputs are there in each multiplexer?
  What size of the multiplexers are needed?
  How many multiplexers are there in the bus?
- Perform arithmetic operations (+42) + (-13) and (-42) – (-13) in binary using signed 2's complement representation for negative numbers.
- Find the product using Booth Multiplication Algorithm.
- a. (9) X (13) b. (9) X (-13) c. (-9) X (13) d. (-9) X (-13)
- Perform the division of 27 and 4 using Division algorithm.
- Design a 4- bit combinational circuit decrementer using 4 full adder circuits.
- Register A holds the 8-bit binary 11011001. Determine the B operand and the logic micro operation to be performed in order to change the value in A to :
  a) 01101101 b) 11111101

- An 8-bit register contains the binary value 10011100. What is the register value after an arithmetic shift right? Starting from the initial number 10011 100, determine the register value after an arithmetic shift left, and state whether there is an overflow.
- Starting from an initial value of R =11011101, determine the sequence of binary values in R after a logical shift-left, followed by a circular shift-right, followed by a logical shift-right and a circular shift-left.
- Design arithmetic logic shift unit that performs different operations on 4 bits.

SKILLS:

- ✓ *Learn different data representations.*
- ✓ *Design digital circuitry for implementing different operations.*
- ✓ *Identify the types of memories and their uses.*
- ✓ *Study various data transfer mechanisms in digital computer and I/O.*

MODULE-2

UNIT-1 **8L+8T+0P=16 Hours**

CPU AND MEMORY ORGANIZATION

Central Processing Unit: General Register Organization, STACK Organization. Instruction Formats, Addressing Modes, Data Transfer and Manipulation, Program Control.

Memory Organization: Memory Hierarchy, Main Memory, Auxiliary Memory, Associative Memory, Cache Memory.

UNIT-2 **8L+8T+0P=16 Hours**

I/O ORGANIZATION

Input-Output Organization: Peripheral Devices, Input-Output Interface, Asynchronous data transfer, Modes of Transfer, Priority Interrupts, Direct Memory Access.

PRACTICES:

- The content of PC in the basic computer is 3AF (all numbers are in hexadecimal). The content of AC is 7EC3. The content of memory at address 3AF is 932E. The content of memory at address 32E is 09AC. The content of memory at address 9AC is 8B9F.

  What is the instruction that will be fetched and executed next?

  Show the binary operation that will be performed in the AC when the instruction is executed.

  Give the contents of registers PC, AR, DR, AC, and IR in hexadecimal and the values of E, I, and the sequence counter SC in binary at the end of the instruction cycle.
- Implement the given expressions into different addressing architectures.

  Y=(A-B)/(C*D + E) b. Y=A-B+C*(D *E+F)
- How many 128 x 8RAM chips are needed to provide a memory capacity of 2048 byte?
- How many lines of the address bus must be used to address 2048 bytes of memory? How many of these lines will be common to all chips?
- How many lines must be decoded for chip select and design the size of the decoders.
- A computer uses RAM chips or 1024 x 1 capacity.

  How many chips are needed, and show the connection of memory capacity 1024 bytes?

  How many chips are needed to provide a memory capacity or 16K bytes? Explain in words how the chips are to be connected to the address bus.
- How many characters per second can be transmitted over a 1200-baud line in each of the following modes? (Assume a character code of eight bits.)

  Synchronous serial transmission.

  Asynchronous serial transmission with two stop bits.

  Asynchronous serial transmission with one stop bit.
- Information is inserted into a FIFO buffer at a rate of m bytes per second. The information is deleted at a rate of n byte per second. The maximum capacity of the buffer is k bytes.

  How long does it take for an empty buffer to fill up when m >n?

  How long does it take for a full buffer to empty when m <n?

  Is the FIFO buffer needed if m = n?

COURSE OUTCOMES:

Upon successful completion of this course, students will have the ability to:

CO No.	Course Outcomes	Blooms Level	Module No.	Mapping with POs
1	Analyze Computer Organization and Computer Architecture, different arithmetic operations.	Analyze	1	1, 2, 12
2	Design different digital circuits required to perform the micro operations.	Apply	1	1, 2, 3, 12
3	Design interface circuits for memory and peripheral, DMA and communication devices. Compare various modes of transfer.	Analyze	2	1, 2, 3, 4, 12
4	Evaluate the performance of a processor and memory in terms of speed, size and cost.	Evaluate	2	1, 2, 12

TEXT BOOKS:

1. M. Morris Mano, “Computer System Architecture”, 3rd Edition update, Pearson, 2017.
2. William Stallings, “Computer Organization & Architecture: Designing for Performance”, 11th Edition, Pearson, 2019.

REFERENCE BOOKS:

1. Carl Hamacher, ZvonkoVranesic, SafwatZaky, “Computer Organization”, 5th Edition, McGraw Hill, 2002.
2. Vincent P. Heuring and Harry F Jordan, “ Computer Systems Design and Architecture “, 2nd edition , Pearson/ Prentice Hall India 2004.
3. David A. Patterson and John L. Hennessy, “Computer Organization and Design-The Hardware/ Software Interface”, ARM Edition, 5th Edition, Elsevier, 2009.