20VL002 - Digital IC Design

Course Outcomes:

CO1: Design CMOS inverters with specified noise margin and propagation delay.
CO2: Implement efficient techniques at circuit level for improving power and speed of digital circuits
CO3: Design a processor meeting timing constraints.
CO4: Design semiconductor memories to improve access times and power consumption.
CO5: Synthesize digital circuit using HDLs.

UNIT – I
CMOS Inverter: Introduction to MOS transistor, V-I Characteristics, Electrical Parameters, Static behavior, switching Threshold, Noise Margins, Robustness revisited, Dynamic behavior: Computing the capacitances, propagation delay, propagation delay from a design perspective, power, energy and energy delay.

UNIT – II
Combinational Logic Design: Introduction, Static CMOS Design: Complementary CMOS, ratioed logic, pass transistor logic dynamic CMOS Design: Dynamic logic, speed and power dissipation of dynamic logic, signal integrity issues in Dynamic design, cascading dynamic gates.

UNIT – III
Sequential Logic Design: Introduction, static latches and registers: The Bi-stability principle, multiplexer based latches, master-slave edge-Triggered register, low-voltage static latches, Static SR Flip-flop, dynamic latches and registers, dynamic transmission, Gate Edge - triggered registers, CMOS NORA-CMOS True single - phase clocked register (TSPCER).

UNIT – IV
Timing Issues in Digital Circuits: Introduction, Timing classification of digital systems, synchronous design, Self-Timed circuit design, synchronizers and arbiters.

UNIT – V
Digital Integrated System Building Blocks: Introduction, Adders, Multipliers, Shifters, Memories, ROM, RAM, Internal structure, ROM 2 D Structure, SRAM, DRAM.

DIGITAL IC DESIGN LAB

List of Experiments

1. Design of Inverter and all logic gates
2. Design and Simulation of Full adder
3. Design and Simulation of Serial Binary Adder, Carry Look Ahead Adder.
4. Design of SRAM and DRAM
5. Design of pseudo logic gates
6. Design of DCVSL logic gates
7. Design of flip flops: SR, D, JK, T
8. Design of edge triggered registers
9. Design of barrel shifter
10. Design of Multiplier

Note: Implementing the above designs on Circuit level/ RTL level in Cadence/Xilinx.

TEXT BOOKS:

1. Jan M. Rabaey, AnanthaChandrakasan and Borivoje Nikolic., Digital Integrated Circuits: A Design Perspective, Second Edition, **Pearson Education India,** 2003
2. Ken Martin, Digital Integrated Circuit Design, Oxford University Press, 1st edition, 1999.

REFERENCE BOOKS:

1. Neil H. E. Weste and D. M. Harris, CMOS VLSI Design, Third Edition, 2010.
2. Sung-Mo Kang, CMOS Digital Integrated Circuits, 3rd Edition, McGraw-Hill, 2003.
3. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia.