

# 20VL013 - PHYSICAL DESIGN AUTOMATION

- CO1 Understand the relationship between design automation algorithms and various constraints posed by VLSI fabrication and design technology.
- CO2 Adapt the design algorithms to meet the critical design parameters
- CO3 Identify layout optimization techniques and map them to the algorithms
- CO4 Develop proto-type EDA tool and test its efficacy.

## UNIT I

VLSI design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and Additional Fabrication, Design styles: full custom, standard cell, gate arrays, field programmable gate arrays, sea of gates and comparison, system packaging styles, multi chip modules.

## UNIT II

Design rules, layout of basic devices, fabrication process and its impact on physical design, interconnect delay, noise and cross talk, yield and fabrication cost.

## UNIT III

Factors, Complexity Issues and NP-hard Problems, Basic Algorithms (Graph and Computational Geometry): graph search algorithms, spanning tree algorithms, shortest path algorithms, matching algorithms, min-cut and max-cut algorithms, Steiner tree algorithms.

Basic Data Structures, atomic operations for layout editors, linked list of blocks, bin based methods, neighbour pointers, corner stitching, multi-layer operations.

## UNIT IV

Graph algorithms for physical design: classes of graphs, graphs related to a set of lines, graphs related to set of rectangles, graph problems in physical design, maximum clique and minimum coloring, maximum k-independent set algorithm, algorithms for circlegraphs.

## UNIT V

Partitioning algorithms: design style specific partitioning problems, group migrated algorithms, simulated annealing and evolution, and Floor planning and pin assignment, Routing and placement algorithms.

## Physical Design Automation Lab

### Cycle 1:

#### 1) Graph algorithms

- 1) Graph search algorithms
  - 1) Depth first search
  - 2) Breadth first search
- 2) Spanning tree algorithm
  - 1) Kruskal's algorithm
- 3) Shortest path algorithm
  - 1) Dijkstra algorithm
  - 2) Floyd-Warshall algorithm
- 4) Steiner tree algorithm

#### 2) Computational geometry algorithm

- 1) Line sweep method
- 2) Extended line sweep method

Cycle 2:

**1) Partitioning algorithms**

- 1) Group migration algorithms
- 1) Kernighan –Lin algorithm
- 2) Extensions of Kernighan-Lin algorithm
- 1) Fiduccias –Mattheyses algorithm
- 2) Goldberg and Burstein algorithm
- 2) Simulated annealing and evolutionary algorithms
- 1) Simulated annealing algorithm
- 2) Simulated evolutionary algorithm
- 3) Metric allocation method

**2) Floor planning algorithms**

- 1) Constraint based methods
- 2) Integer programming based methods
- 3) Rectangular dualization based methods
- 4) Hierarchical tree based methods
- 5) Simulated evolutionary algorithms
- 6) Time driven Floor planning algorithms

**3) Routing algorithms**

- 1) Two terminal algorithms
- 1) Maze routing algorithms
- 1) Lee's algorithm
- 2) Soukup's algorithm
- 3) Hadlock algorithm
- 2) Line-Probe algorithm
- 3) Shortest path based algorithm
- 2) Multi terminal algorithm
- 1) Stenier tree based algorithm
- 1) SMST algorithm

**Text Books:**

1. Naveed Shervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwer Academic, 1999.
2. Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2008