IV Year B.Tech. ECE II - Semester

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EC422 VLSI TESTING & VALIDATION
(Dept. Elective – VI)

Course Description & Objectives:

This course includes the testing of VLSI circuits and their validation. Each VLSI circuits has inbuilt testing process and validation. To make the students involve in the theory and practice of VLSI testing and validations and to introduce advanced techniques for efficiently testing and validating the VLSI design.

Course Outcomes:

Upon successful completion of this course, students should be able to:

a. Effectively test VLSI systems using existing test methodologies, equipments, and tools.
b. Define a methodology to test the combinational and sequential circuits.
c. To construct a Design for Testability (DFT) algorithm for VLSI Circuits.
d. Able to design testing circuits for VLSI Circuits.
e. Able to design different test algorithms .

UNIT I - Introduction to VLSI Testing :

Introduction - VLSI Testing Process And Test Equipment - Test Economics and Product Quality – Fault Molding-Logic and Fault Simulation.

UNIT II -Test Generation for Combinational and Sequential Circuits :

Test generation for combinational logic circuits - Testable combinational logic circuit design - Test generation for sequential circuits - design of testable sequential circuits

UNIT III - Advanced Testing :

Memory Test- DSP-based analog and mixed signal test- Model based analog and mixed signal test - Delay Test - IDDQ Test.

UNIT IV - Design For Testability :

Design for Testability - Ad-hoc design - Storage cells for scan designs - Generic scan based design - System level DFT approaches.

UNIT V - Self Test and Test Algorithms :

Built-In Self Test - Test pattern generation for BIST - Circular BIST - BIST Architectures - Testable Memory Design - Test algorithms - Test generation for Embedded RAMs.

TEXT BOOKS :

1. Viswani D.Agarval Michael L.Bushnell, “Essentials of Electronic Testing for DigitalMemory & Mixed Signal VLSI Circuit “, Kluwer Academic Publications, 2000.
2. L. T. Wang, C. W. Wu, and X. Wen, VLSI Test Principles and Architectures, Morgan

REFERENCE BOOKS :

1. Kaufmann Morgan Kaufmann Publishers, 2006 M. Abramovici, M.A. Breuer and A.D. Friedman, “Digital Systems and Testable Design”, Jaico Publishing House, 2002.
2. Alfred L.Crouch “Design for Test for Digital IC’s And Embedded Core Systems “, -PHI 1999.