17VL010 NANO ELECTRONICS

Hours Per Week :

L	T	P	C
4	-	-	4

Total Hours :

L	T	P
60	-	-

WA/RA	SSH/HSH	CS	SA	S	BS
15	30	-	5	5	-

Course Objectives:

- To acquire knowledge about fundamental quantum mechanics.
- To study about architecture and operations of different nano structures.
- To comprehend the low dimension, high speed and low power design techniques and methodologies.

Course Outcomes:

Upon successful completion of this course student should be able to:

- To explain challenges due to scaling on CMOS devices, VLSI circuit design and fundamental limits of operation.
- To analyze and explain working of novel MOS based silicon devices and various multi gate devices.
- To analyze and explain working of SOI devices and their performance comparison with Silicon devices
- To understand the underlying concepts by setting up and solving the Schrödinger equation for different types of potentials in one dimension as well as in 2 or 3 dimensions for specific cases.
- To understand nanoelectronic systems and building blocks such as: low dimensional semiconductors, heterostructures, carbon nanotubes, quantum dots, nanowires etc.

SKILLS:

- knowledge about Quantum structures.
- Utilise the nano scale transistors for current applications.

UNIT - I

Challenges going to sub-100 nm MOSFETs – Oxide layer thickness, tunneling, power density, non-uniform dopant concentration, threshold voltage scaling, lithography, hot electron effects, sub-threshold current, velocity saturation, interconnect issues, fundamental limits for MOS operation. High-K gate dielectrics, effects of high-K gate dielectrics on MOSFET performance.

UNIT - II

Novel MOS-based devices – Multiple gate MOSFETs, Silicon-on-nothing, Silicon-on-insulator devices, FD SOI, PD SOI, FinFETs, vertical MOSFETs, strained Si devices 34.

UNIT - III

Hetero structure based devices – Type I, II and III Heterojunction, Si-Geheterostructure, hetero structures of III-V and II-VI compounds - resonant tunneling devices, MODFET/HEMT.

UNIT - IV

Carbon nanotubes based devices – CNFET, characteristics, Spin-based devices – spinFET, characteristics.

UNIT - V

Quantum structures – quantum wells, quantum wires and quantum dots, Single electron devices – charge quantization, energy quantization, Coulomb blockade, Coulomb staircase, Bloch oscillations

ACTIVITIES:

- Using cadence tool, code should be written for FinFET and CNTFET, also simulated.
- And schematics were drawn using MOSFETs.

TEXT BOOKS

1. Mircea Dragoman and Daniela Dragoman, Nanoelectronics – Principles & devices, Artech House Publishers, 2005.
2. Karl Goser, Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices, Springer 2005.
3. Mark Lundstrom and Jing Guo, Nanoscale Transistors: Device Physics, Modeling and Simulation, Springer, 2005.
4. Vladimir V Mitin, Viatcheslav A Kochelap and Michael A Stroscio, Quantum heterostructures, Cambridge University Press, 1999.

REFERENCE BOOKS

1. S.M. Sze (Ed), High speed semiconductor devices, Wiley, 1990.
2. ManijehRazeghi, Technology of Quantum Devices, Springer, ISBN 978-1-4419-1055-4.
3. H.R. Huff and D.C. Gilmer, High Dielectric Constant Materials for VLSI MOSFET Applications, Springer 2005, ISBN 978-3-540-21081-8 , (Available on NITC intranet in Springer eBook section)
4. B.R. Nag, Physics of Quantum Well Devices, Springer 2002, ISBN 978-0-7923-6576-1, (Available on NITC intranet in Springer eBook section).
5. E.Kasper, D.J. Paul, Silicon Quantum Integrated Circuits Silicon-Germanium Heterostructures Devices: Basics and Realisations, Springer 2005, ISBN 978-3-540-22050-3, (Available on NITC intranet in Springer eBook section).